AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1-8 (canceled).

9. (original): A switch connector which is adaptable to a computer system including, a memory bus, at least one memory slot and an electric load, wherein:

said switch connector couples one of a plurality of signal lines of said memory bus to one of a plurality of module pins of a memory module, in a case where said memory module is inserted in said at least one memory slot; and

said switch connector couples the one of said plurality of signal lines of said memory bus to said electric load, in a case where said memory module is not inserted in said at least one memory slot.

10. (original): The switch connector according to claim 9, wherein

said switch connector is disposed inside said at least one memory slot.

11. (original): A switch connector which is adaptive to a computer system including, a memory bus, at least one memory slot and an electrical load, comprising:

a first connector pin which is coupled to one of a plurality of signal lines of said memory bus; and

a second connector pin which is coupled to said electric load, and wherein

said switch connector provides electric contact between said first connector pin and said second connector pin, in a case where a memory module is not inserted in said at least one memory slot, and

said switch connector insulates said first connector pin from said second connector pin, in a case where said memory module is not inserted in said at least one memory slot.

12. (original): The switch connector according to claim 11, wherein:

one end of said first connector pin is fixed on a casing of said at least one memory slot; and

other end of said first connector pin provides flexible electric contact with said second connector pin or with one of a plurality of module pins of said memory module.

13. (original): A method of controlling operations of a computer system including a plurality of memory slots, comprising:

arranging a plurality of memory connectors on each of said plurality of memory slots;

coupling a plurality of bus lines respectively to said plurality of memory connectors;

coupling at least one impedance matching circuit to at least one of said plurality of memory connectors;

coupling said plurality of bus lines to a memory module, in at least one of said plurality of memory slots in which the memory module is inserted; and

coupling said at least one impedance matching circuit to at least one of said plurality of bus lines, in at least one of said plurality of memory slots in which the memory module is not inserted.

14. (original): The method according to claim 13, further comprising:

coupling said plurality of bus lines respectively to first-type connector pins included in each of said plurality of memory connectors;

coupling said at least one impedance matching circuit to at least one of second-type connector pins included in at least one of said plurality of memory connectors;

providing electric contact between said first-type connector pins and module pins of the memory module, in the at least one of said plurality of memory slots in which the memory module is inserted; and

providing electric contact between said first-type connector pins and said second-type connector pins, in at least one of said plurality of memory slots in which the memory module is not inserted.